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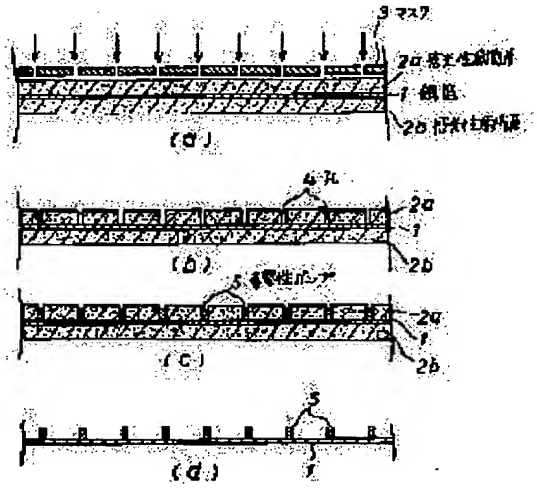
(54) MANUFACTURE OF MOUNTING PRINTED WIRING BOARD

(57)Abstract:
PURPOSE: To obtain a mounting wiring board equipped with fine terminals accurately located at prescribed positions by a method wherein the terminals electrically connected to the input/output terminals of electronic parts which are mounted on the board are selectively grown and formed through a plating method on the tips of conductive bumps that penetrate through an insulating layer.
CONSTITUTION: Photosensitive resist films 2a and 2b are pasted on both the sides of an electrolytic copper foil 1 respectively and irradiated with light rays through the intermediary of a mask 3, and holes 4 are provided in the resist film 2a by development. Thereafter the copper foil 1 is dipped into a copper electroplating solution and subjected to copper electroplating, whereby an electrolytic copper foil 1 where protrudent conductive bumps 5 are formed on one main surface is obtained. Then, a synthetic resin sheet, an aluminum foil, and a kraft paper are laminated on the electrolytic copper foil 1, which is pressed by a hot press into a laminate where the tips of the conductive bumps 5 are exposed on the outer surface of the synthetic resin sheet penetrating through it. Thereafter, a wiring is patterned by selective etching, etching resist is removed, and thus a mounting wiring board is obtained.



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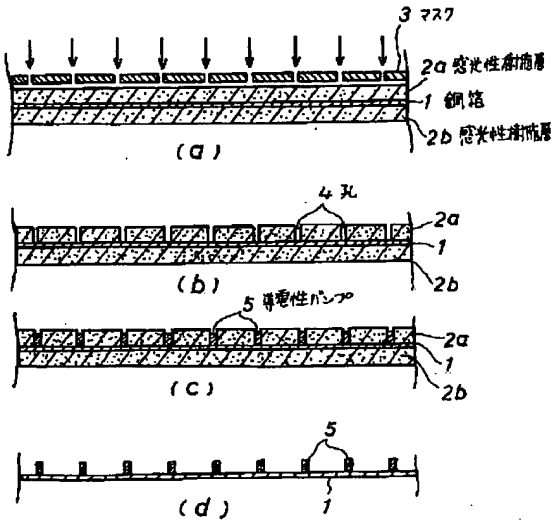
(54)【発明の名称】　実装用印刷配線板の製造方法

(57)【要約】

【目的】　信頼性の高い高密度配線および高密度実装を可能とした実装用配線板の製造方法の提供を目的とする。

【構成】　導電性金属箔１の主面に感光性レジスト層2a，2bを配設する工程と、前記感光性レジスト層2a，2bを選択的に露光し、現像処理して導電性金属箔１面を選択的に露出させる工程と、前記露出した導電性金属箔１面上に導電性金属をめっき成長させ、導電性バンプ５を形成する工程と、前記導電性バンプ５形成面の感光性レジスト層2a，2bを剥離・除去する工程と、前記導電性金属箔１の導電性バンプ５形成面に合成樹脂系シート６を重ね積層する工程と、前記積層体を加圧し、導電性バンプ５先端部を絶縁性合成樹脂シート６の厚さ方向に貫挿・露出させて接続用端子部９を形成する工程と、前記導電性金属箔１を選択的にエッチング除去し、配線パターニングする工程とを具備して成ることを特徴とする。



1

【特許請求の範囲】
【請求項１】　導電性金属箔の主面に感光性レジスト層を配設する工程と、
前記感光性レジスト層を選択的に露光し、現像処理して導電性金属箔面を選択的に露出させる工程と、
前記露出した導電性金属箔面上に導電性金属をめっき成長させ、導電性バンプを形成する工程と、
前記導電性バンプ形成面の感光性レジスト層を剥離・除去する工程と、
前記導電性金属箔の導電性バンプ形成面に合成樹脂系シートを重ね積層する工程と、
前記積層体を加圧し、導電性バンプ先端部を絶縁性合成樹脂シートの厚さ方向に貫挿・露出させて接続用端子部を形成する工程と、
前記導電性金属箔を選択的にエッチング除去し、配線パターニングする工程とを具備して成ることを特徴とする実装用配線板の製造方法。
【請求項２】　配線パターン形成主面に感光性レジスト層を配設する工程と、　前記感光性レジスト層を選択的に露光し、現像処理して配線パターン面を選択的に露出させる工程と、
前記露出した配線パターン面上に導電性金属をめっき成長させ、導電性バンプを形成する工程と、
前記導電性バンプ形成面の感光性レジスト層を剥離・除去する工程と、
前記配線パターンの導電性バンプ形成面に合成樹脂系シートを重ね積層する工程と、
前記積層体を加圧し、導電性バンプ先端部を絶縁性合成樹脂シートの厚さ方向に貫挿・露出させて接続用端子部を形成する工程とを具備して成ることを特徴とする実装用配線板の製造方法。
【請求項３】　貫挿・露出した接続用端子部面を低接触抵抗性金属のめっき層で被覆することを特徴とする請求項１もしくは請求項２記載の実装用配線板の製造方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は実装用配線板の製造方法に係り、さらに詳しくは、実装電子部品の入出力端子と接続する配線パターンの端子部が実装面に導出された実装用配線板の製造方法に関する。
【０００２】
【従来の技術】たとえば半導体素子など、各種の電子部品を配線板に搭載・実装して成る実装回路装置は、電子機器類の回路部品として広く実用に供せられている。そして、この種の実装回路装置の構成には、回路の高密度化もしくはコンパクト化などの要求に対応して、いわゆる多層型配線板が利用されている。より具体的には、たとえばコンピュータなどの電子回路では、半導体素子間に高速な信号伝搬ができるように、配線長を短くする高密度実装手段が採られている。つまり、半導体素子をベアチップのまま実装して実装面積を小さくする一方、配線幅の小さな配線板を用いて実装密度を上げながら、配線長を短くして回路の高密度化などに対応している。

2

【０００３】ところで、前記多層型配線板は、一般的に、次のような手段で製造されている。すなわち、絶縁性基板の両面に張られた銅箔を、それぞれ配線パターニングした後、その配線パターニング面上に絶縁シート（たとえばプリプレグ層）を介して銅箔を積層，配置し、加熱加圧により一体化する。次いで、前記積層体に、たとえばドリルなどで孔明け加工を施した後、化学メッキ法で孔の内壁面を金属層化し、さらに電気メッキで厚付けして、内層配線パターンと外層配線パターンとの配線層間の電気的接続を行う。その後、表面銅箔について、端子部（接続用パッド）を含む配線パターニングを行い多層型配線板を得ている。なお、より配線パターン層の多い多層型配線板の場合は、中間に介挿させる両面型配線板数を増加する方式で製造されている。
【０００４】さらに、前記とは構成の異なる多層型配線板として、たとえばセラミックスを層間絶縁体層とした配線基板面に、たとえばポリイミド系樹脂を層間絶縁体層とする薄膜多層配線層を積層・一体化した構成の配線板も実装用に供せられている。　また、上記によって製造された多層型印刷配線板に、半導体素子（ LSI）をベアチップのまま実装して高密度実装を図る場合は、ベアチップの入出力端子側に半田でバンプを設け、この半田バンプを介して多層型印刷配線板面の端子部（パッド）と接続している。
【０００５】
【発明が解決しようとする課題】しかしながら、上記半田バンプを介したベアチップの実装手段では、実装するベアチップの入出力端子のサイズ合わせた微小サイズの半田バンプが要求されるので、半田バンプの形成が煩雑化するばかりでなく、半田バンプの形状・サイズおよび位置・精度などの点から歩留まりにも問題がある。一方、配線板においては、高密度実装化に対応して、配線幅の狭小化だけでなく、ベアチップの入出力端子を接続する端子部（パッド）の微小化もしくは端子部（パッド）間の狭小化が要求される。そして、この多層型配線板においては、前記配線密度の向上、および実装密度の向上を考慮すると、配線パターン層間を連結するスルホール径にも自ずから限界があり、直径0.10mm程度にスルホール径を設定する場合、たとえばNCドリルマシン加工を適用し得ないので、別途、新たな加工装置もしくは加工手段が要求されることになる。いずれにしても、従来知られている構成の多層型配線板、もしくは従来の製造手段で形成される多層型配線板の場合は、実装回路装置の高密度化やコンパクト化のうえで問題がある。
【０００６】本発明は、上記事情に対処してなされたもので、信頼性の高い高密度配線および高密度実装を可能とした実装用配線板の製造方法の提供を目的とする。

【０００７】

【課題を解決するための手段】本発明に係る第１の実装用配線板の製造方法は、導電性金属箔の主面に感光性レジスト層を配設する工程と、前記感光性レジスト層を選択的に露光し、現像処理して導電性金属箔面を選択的に露出させる工程と、前記露出した導電性金属箔面上に導電性金属をめっき成長させ、導電性バンプを形成する工程と、前記導電性バンプ形成面の感光性レジスト層を剥離・除去する工程と、前記導電性金属箔の導電性バンプ形成面に合成樹脂系シートを重ね積層する工程と、前記積層体を加圧し、導電性バンプ先端部を絶縁性合成樹脂シートの厚さ方向に貫挿・露出させて接続用端子部を形成する工程と、前記導電性金属箔を選択的にエッチング除去し、配線パターニングする工程とを具備して成ることを特徴とする。また、本発明に係る第２の実装用配線板の製造方法は、配線パターン形成主面に感光性レジスト層を配設する工程と、前記感光性レジスト層を選択的に露光し、現像処理して配線パターン面を選択的に露出させる工程と、前記露出した配線パターン面上に導電性金属をめっき成長させ、導電性バンプを形成する工程と、前記導電性バンプ形成面の感光性レジスト層を剥離・除去する工程と、前記配線パターンの導電性バンプ形成面に合成樹脂系シートを重ね積層する工程と、前記積層体を加圧し、導電性バンプ先端部を絶縁性合成樹脂シートの厚さ方向に貫挿・露出させて接続用端子部を形成する工程とを具備して成ることを特徴とする。

【０００８】さらに、上記製造方法において、積層体の加圧により合成樹脂系シートを貫挿・露出した接続用端子部面を低接触抵抗性金属のめっき層で被覆することが好ましい。

【０００９】本発明においては、銅など導電性金属の選択的なメッキによって、導電性バンプが形成される。そして、この選択的なメッキを行うためのマスク材としては、高精度で微小な、さらには微小ピッチな導電性バンプの任意な形成を可能とするために感光性樹脂が選ばれ、この感光性樹脂の配設は感光性樹脂フィルムの張り合わせ、もしくは感光性樹脂溶液の塗布・乾燥などで行われる。

【００１０】また、前記導電性金属のめっきにより形成する突起状（たとえば円錐状もしくは柱状体など）の導電性バンプは、前記感光性樹脂層が成すマスクの厚さや、マスクに設けられた孔の径，および分布などによっ決まるので、形成する貫挿型の端子部（パッド）および配線パターン層間の接続部の構成に応じて適宜設定される。

【００１１】前記突起状の導電性バンプの先端部が貫挿され、端子部および層間接続部を形成する合成樹脂系シートとしては、たとえば熱可塑性樹脂フイルム（シート）が挙げられ、その厚さは25～ 300μｍ 程度が好ましい。ここで、熱可塑性樹脂シートとしては、たとえばポリカーボネート樹脂，ポリスルホン樹脂，熱可塑性ポリイミド樹脂，４フッ化ポリエチレン樹脂，６フッ化ポリプロピレン樹脂，ポリエーテルエーテルケトン樹脂などのシート類が挙げられる。また、硬化前状態に保持される熱硬化性樹脂シートとしては、エポキシ樹脂，ビスマレイミドトリアジン樹脂，ポリイミド樹脂，フェノール樹脂，ポリエステル樹脂，メラミン樹脂，あるいはブタジェンゴム，ブチルゴム，天然ゴム，ネオプレンゴム，シリコーンゴムなどの生ゴムのシート類が挙げられる。これら合成樹脂は、単独でもよいが絶縁性無機物や有機物系の充填物を含有してもよく、さらにガラスクロスやマット、有機合成繊維布やマット、あるいは紙などの補強材と組み合わせて成るシートであってもよい。

【００１２】また、前記導電性バンプの先端部を合成樹脂系シート表面に貫挿・露出させ、端子部（パッド）を形成するに当たっては、次のような手段を採ることが好ましい。すなわち、突起状の導電性バンプを形設した基体面へ、合成樹脂系シート主面を対接させて積層配置し、この積層体の両側に当て板として寸法や変形の少ない、たとえばステンレス板，真鍮板などの金属板、たとえばポリイミド樹脂板（シート），ポリテトラフロロエチレン樹脂板（シート）などの耐熱性樹脂板を配置して加圧して、突起状の導電性バンプ先端側を合成樹脂系シートの厚さ方向に貫挿させることにより形成できる。

【００１３】

【作用】本発明に係る実装用配線板の製造方法によれば、実装する電子部品の入出力端子と電気的に接続される端子部（パッド）は、いわゆるめっき法によって選択的に成長・形成され、かつ絶縁体層を貫挿した導電性バンプの先端部で形成されている。つまり、端子部（パッド）は、埋め込み導出形で配線板面に露出される構成を採り、また高精度の寸法，形状（たとえば高さのばらつきは± 2μｍ 程度）に形成されるばかりでなく、 300μｍ 程度以下（たとえば 100μｍ 程度）のピッチで配設し得る。そして、前記導電性バンプを、微細な形状および微小なピッチで設置し得ることに伴って、配線密度および実装密度の向上も併せて図られた配線板が得られることになる。しかも、配線板面にスルホールが存在しないため、少なくともその分配線領域および実装領域の低減も解消することになり、前記配線密度および実装密度の向上がさらに助長されることになり、信頼性の高い実装用配線板を歩留まりよく提供し得る。

【００１４】

【実施例】以下、図１ (a)～ (d)、図２ (a)～ (c)、図３ (a)， (b)、図４ (a)～ (c)、図５ (a)， (b)および図６ (a)～ (c)を参照して本発明の実施例を説明する。

【００１５】実施例１

図１ (a)～ (d)および図２ (a)～ (c)はこの実施例による実装用配線板の製造方法の態様例を模式的に示したものである。

【００１６】先ず、印刷配線板の製造に使用されている厚さ18μm の電解銅箔、および厚さ150μm の感光性樹脂フイルム（商品名：Photec SR-3000EB-22 日立化成KK製）を用意した。そして、図１ (a)に断面的に示すごとく、前記電解銅箔１の両面に、前記感光性樹脂（感光性レジスト）フイルム2a，2bを、それぞれ張り合わせた後、マスク３を介して光を感光性レジストフイルム2aに照射（選択的露光）した。次いで、前記選択的露光した感光性レジストフイルム2a，2bについて現像処理を施して、図１ (b)に断面的に示すように、感光性レジストフイルム2aに直径約75μm の孔４を設けた。

【００１７】その後、前記電解銅箔１を陰極として、電気銅めっき液（商品名：KC500 ジャパンエナジーKK製）中に浸漬し、電気銅めっき処理を行い、図１ (c)に断面的に示すごとく、前記感光性レジストフイルム2aの孔４内（電解銅箔１の選択的な露出面）に、高さ 130μm 程度の銅を成長させた。前記めっき処理終了後、マスクとして機能させた感光性樹脂フィルム2a，2bを剥離して、図１ (d)に断面的に示すように、突起状の導電性バンプ５群が一主面に形成された電解銅箔１を得た。次に、前記電解銅箔１の突起状導電性バンプ５群形成面に、図２ (a)に断面的に示すごとく、厚さ50μm の合成樹脂シート６、たとえばテフロン樹脂－ガラスクロス系プリプレグ、および図示しないアルミ箔，クラフト紙を積層配置した。この積層体を、 180℃に保持した熱プレス機の熱板間にセットし、約1.96×10^6 Paで加圧してそのまま15分間保持し、図２(b) に断面的に示すような、導電性バンプ５先端部が合成樹脂シート６層を貫挿して他の面に露出した積層板を得た。その後、前記積層板の電解銅箔１面にエッチングレジストを印刷し、その電解銅箔１の選択的なエッチングを行って、配線パターニング７してから、前記エッチングレジストをアルカリ水溶液で剥離除去して、図２(c) に断面的に示すような、実装用配線板８を得た。

【００１８】前記実装用配線板８においては、図２ (c)に断面的に示すごとく、一方の主面（表面）には、導電性バンプ５の先端部が端子部（パッド） ９として露出し、他方の主面（裏面）には、端子部９と接続する配線パターン７が形設された構成を成している。そして、前記端子部９所定位置に設定されており、図３ (a)に断面的、また図３ (b)に平面透視的に示すように、たとえば LSI（半導体）ベアチップ10の入出力端子 10aと確実に対接され、金属間の接合（金属同士の結合，金属常温接合を含む）によって安定した電気的な接続がなされた。

【００１９】実施例２

図４ (a)～ (c)は、この実施例による実装用配線板の製造方法の態様例を模式的に示したものである。

【００２０】先ず、印刷配線板の製造に使用されている厚さ18μm の電解銅箔、および厚さ150μm の感光性樹脂フイルム（商品名：Photec SR-3000EB-22 日立化成KK製）を用意した。そして、前記電解銅箔１の両面に、前記感光性樹脂（感光性レジスト）フイルム2a，2bを、それぞれ張り合わせた後、マスクを介して光を感光性レジストフイルム2aに照射（選択的露光）した。次いで、前記選択的露光した感光性レジストフイルム2a，2bについて現像処理を施して、感光性レジストフイルム2aに直径約75μm の孔４を設けた。

【００２１】その後、前記電解銅箔１を陰極として、電気銅めっき液（商品名：KC500 ジャパンエナジーKK製）中に浸漬し、電気銅めっき処理および金めっき処理を順次行い、図４ (a)に断面的に示すごとく、前記感光性レジストフイルム2aの孔４内（電解銅箔１の選択的な露出面）に、高さ 130μm 程度の銅5aを成長させ、さらにその上に高さ15μm 程度の金5bを積層させた。前記めっき処理終了後、マスクとして機能させた感光性樹脂フィルム2a，2bを剥離して、銅5aおよび金5bが積層された形の突起状導電性バンプ５群が一主面に形成された電解銅箔１を得た。

【００２２】次に、前記電解銅箔１の突起状導電性バンプ５群形成面に、厚さ50μm の合成樹脂シート３、たとえばテフロン樹脂－ガラスクロス系プリプレグ、およびアルミ箔やクラフト紙を積層配置した。この積層体を、180℃に保持した熱プレス機の熱板間にセットし、約1.96×10^6 Paで加圧してそのまま15分間保持し、導電性バンプ５先端部が合成樹脂シート６層を貫挿して他の面に露出した積層板を得た。 その後、前記積層板の電解銅箔１面にエッチングレジストを印刷し、その電解銅箔１の選択的なエッチングを行って、配線パターニング７してから、前記エッチングレジストをアルカリ水溶液で剥離除去して、実装用配線板８を得た。

【００２３】前記実装用配線板８においては、図４ (b)に断面的に示すごとく、一方の主面（表面）には、導電性バンプ５の先端部が端子部（パッド） ９として露出し、他方の主面（裏面）には、端子部９と接続する配線パターン７が形設された構成を成している。そして、前記端子部９高精度に所定位置に設定されており、図４ (c)に断面的に示すように、たとえば LSI（半導体）ベアチップ10の入出力端子 10aと確実に対接され、金属間の接合によって安定した電気的な接続がなされた。

実施例３

図５ (a)および (b)は、この実施例による実装用配線板の製造方法の他の態様例を模式的に示す断面図である。

【００２４】先ず、印刷配線板の製造に使用されている厚さ18μm の電解銅箔、ポリマータイプの銀系ペースト（商品名：ケミタイトMS-89.東芝ケミカルKK製）、厚さ100μm のステンレス鋼板の所定位置に 0.1㎜径の孔を明けて成るメタルマスクをそれぞれ用意した。そして、前記電解銅箔面に、メタルマスクを位置決め配置して、銀系ペーストを印刷して突起状の導電性バンプを、ほぼ方形に最小で 0.3㎜程度のピッチで被着形成した。前記

印刷した導電性バンプが乾燥後、同一のメタルマスクを用いて同一位置に再度印刷する方法を４回繰り返し、高さ60～ 100μmの略円錐状の導電性バンプ形成した。

【００２５】次いで、前記電解銅箔の導電性バンプ形成面側に、厚さ50μm の合成樹脂シート、たとえばテフロン樹脂－ガラスクロス系プリプレグを介して、厚さ18μm の電解銅箔を積層配置した。この積層体を、 180℃に保持した熱プレス機の熱板間にセットし、約1.96×10^6 Paで加圧してそのまま15分間保持し、図４(b) に断面的に示すような、導電性バンプの先端部が合成樹脂シート層を貫挿して対向する電解銅箔面との間が電気的に接続された積層板を得た。

【００２６】次いで、前記積層板の両電解銅箔１面にエッチングレジストを印刷し、その電解銅箔１の選択的なエッチングを行って、配線パターニングしてから、前記エッチングレジストをアルカリ水溶液で剥離除去して、両面型配線板を得た。この両面型配線板の一方の配線パターン面の所定位置に、前記手法にしたがって銀ペースト系の導電性バンプの形成、たとえばテフロン樹脂－ガラスクロス系プリプレグを介しての厚さ18μm の電解銅箔の積層一体化、この電解銅箔の配線パターニングを繰り返して、図５ (a)に断面的に示すような積層配線板11を作成した。

【００２７】前記作成した積層配線板11の導電性バンプ５′形成面に、厚さ50μm のたとえばテフロン樹脂－ガラスクロス系プリプレグを介して、前記図４ (b)に図示した実装用配線板８を積層配置した。この積層体を、 180℃に保持した熱プレス機の熱板間にセットし、約1.96×10^6 Paで加圧してそのまま15分間保持し、導電性バンプ５′先端部が合成樹脂シート６層を貫挿して実装用配線板８の配線パター７に電気的に接続するとともに、実装用配線板８および積層配線板11が積層一体化して成る多層型の実装用配線板12を得た。

【００２８】前記多層型の実装用配線板12においては、一方の主面（表面）に導電性バンプ５の先端部が端子部（パッド）９として露出した構成を成している。そして、前記端子部９所定位置に精度よく配設されているので、たとえば LSI（半導体）ベアチップの入出力端子にが確実に対接され、金属間の接合によって安定した電気的な接続がなされた。

【００２９】実施例４

図６ (a)～ (c)はこの実施例による実装用配線板の製造方法の態様例を模式的に示したものである。

【００３０】先ず、印刷配線板の製造に使用されている厚さ18μm の電解銅箔、および厚さ150μm の感光性樹脂フイルム（商品名：Photec SR-3000EB-22 日立化成KK製）を用意した。そして、前記電解銅箔１の両面に、前記感光性樹脂（感光性レジスト）フイルム2a，2bを、それぞれ張り合わせた後、マスク３を介して光を感光性レジストフイルム2aに照射（選択的露光）した。なお、この選択的露光処理においては、テスターのプローブ接触用導体バンプ13を周辺部に設置するための露光も併せて行った。

【００３１】次いで、前記選択的露光した感光性レジストフイルム2a，2bについて現像処理を施して、感光性レジストフイルム2aに直径約75μm の孔４，４′を設けた。

【００３２】その後、前記電解銅箔１を陰極として、電気銅めっき液（商品名：KC500 ジャパンエナジーKK製）中に浸漬し、電気銅めっき処理および金めっき処理を順次行い、図６ (a)に断面的に示すごとく、前記感光性レジストフイルム2aの孔４内（電解銅箔１の選択的な露出面）に、高さ 130μm 程度の銅5aを成長させ、さらにその上に高さ15μm 程度の金5bを積層させ、また孔４′内（同じく電解銅箔１の選択的な露出面）に高さ 150～ 200μm 程度の銅5aを成長させ、さらにその上に、高さ15μm 程度の金5bを積層させた。前記めっき処理終了後、マスクとして機能させた感光性樹脂フィルム2a，2bを剥離して、銅5aおよび金5bが積層された形の突起状導電性バンプ５，13群が一主面に形成された電解銅箔１を得た。

【００３３】次いで、図６ (b) に断面的に示すごとく、前記電解銅箔１の導電性バンプ５，13形成面側に、基板本体を成す厚さ50μm のテフロン樹脂－ガラスクロス系プリプレグ６を積層配置した。この積層体を、 180℃に保持した熱プレス機の熱板間にセットし、約1.96×10^6 Paで加圧してそのまま15分間保持し、導電性バンプ５，13の先端部が合成樹脂シート６層を貫挿して他の面に露出した積層板を得た。

【００３４】さらに、前記積層板の他面に貫挿・露出している導電性バンプ５，13のうち、高さの高い導電性バンプ13をプレス機で押し潰し加工した。次いで、前記積層板の電解銅箔１面にエッチングレジストを印刷し、その電解銅箔１の選択的なエッチングを行って、配線パターニングしてから、前記エッチングレジストをアルカリ水溶液で剥離除去して、図６ (c) に断面的に示すような、実装用配線板８′を得た。

【００３５】前記構成の実装用配線板では、実装するベアチップ10の入出力端子 10aと接続する端子部９に電気的に接続している端子13′が、周辺部に導出されているため、ベアチップ10を搭載・実装した後、前記周辺部に導出させた端子13′を利用して、搭載・実装したベアチップ10の良，不良のテストを容易に行うことが可能である。つまり、テスターのプローブをベアチップ10の入出力端子 10aに直接接触させずとも、実装したベアチップ10の特性調査を容易かつ確実に行うことができ、また、導電性バンプ５，13が形成する端子部９および端子13′間を接続する配線パター７の設計によっては、複数個のテスターのプローブでの特性評価も可能である。 なお、本発明は上記実施例に限定されるものでなく、発明

の趣旨を逸脱しない範囲でいろいろの変形を採り得る。たとえば、配線パターン層間の絶縁体としてはテフロン樹脂－ガラスクロス系の代わりに、ポリイミド樹脂やポリサルホン樹脂などを用いてもよい。

【００３６】

【発明の効果】上記実施例の説明などからも明らかのように、本発明に係る実装用配線板の製造方法によれば、所定位置に精度よく、また微小な端子部（パッド）を備えた構成を採った実装用配線板を容易に得ることが可能となる。たとえば、前記端子部の高さのばらつきも± 2 μm 程度以下であり、端子部における接続抵抗も 0.1Ω 以下で、さらに端子部を 100μm 程度のピッチで配設し得る。そして、前記実装用配線板における端子部の設定位置や形状の高精度化により、たとえばベアチップの対応する入出力端子との位置合わせ，接続も確実に行い得るので、信頼性の高い実装回路装置の提供が可能となる。また、前記端子部の表面導出は、導電性バンプの貫挿で、いわゆる埋め込み形であるため、スルホール穿設やスルホールめっきなど煩雑な加工作業が不要となるばかりでなく、前記スルホールによる配線領域および実装領域の制約も低減されるので、高密度の配線化および実装化が図られる。

【図面の簡単な説明】

【図１】本発明に係る実装用配線板の製造方法例を模式的に示すもので、 (a)は銅箔面に設けた感光性樹脂層の選択的な露光状態を示す断面図、 (b)は現像した状態を示す断面図、 (c)は露出させた銅箔面にめっき処理し突起状の導電性バンプを成長させた状態を示す断面図、 (d)は感光性樹脂層銅箔を剥離・除去した状態を示す断面図。

【図２】本発明に係る実装用配線板の製造方法例を模式的に示すもので、 (a)は突起状の導電性バンプを設けた銅箔面に合成樹脂系シートを配置した状態を示す断面図、 (b)は導電性バンプ先端部が合成樹脂系シートを挿

通した状態を示す断面図、 (c)は銅箔を配線パターニングした状態を示す断面図。

【図３】本発明に係る実装用配線板に LSIベアチップを実装した態様例を模式的に示すもので、 (a)は要部断面図、 (b)は要部平面的な透視図。

【図４】本発明に係る実装用配線板の製造方法の他の実施態様例を模式的に示すもので、 (a)は露出させた銅箔面にめっき処理し突起状の導電性バンプを成長させた状態を示す断面図、 (b)は実装用配線板の断面図、 (c)はLSIベアチップを実装した状態を示す断面図。

【図５】本発明に係る実装用配線板の別の製造方法例を模式的に示すもので、 (a)は突起状の導電ペーストで導電性バンプを設け、この導電性バンプで配線層間を節即した構成の積層配線板の要部断面図、 (b)は (a)に図示した積層配線板と図４ (b)に図示した実装用配線板とを積層一体化して成る多層型実装用配線板の要部断面図。

【図６】本発明に係る実装用配線板のさらに別の製造方法例を模式的に示すもので、(a)は露出させた銅箔面にめっき処理し突起状の導電性バンプを成長させた状態を示す断面図、 (b)は突起状の導電性バンプを設けた銅箔面に合成樹脂系シートを配置した状態を示す断面図、 (c)は銅箔を配線パターニングした状態を示す断面図。

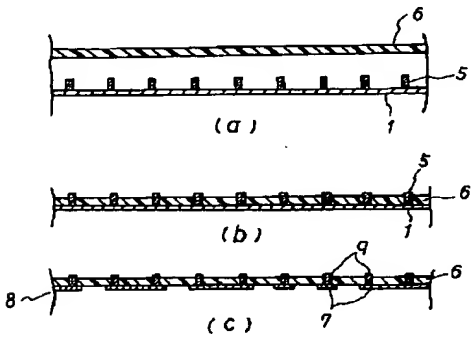
【符号の説明】

１……電解銅箔　　2a，2b……感光性樹脂層　　３……マスク　　４……マスク孔　　５，５′，13……導電性バンプ　　６……合成樹脂系シート（プリプレグ層）　　７……配線パターン　　８，８′……実装用配線板

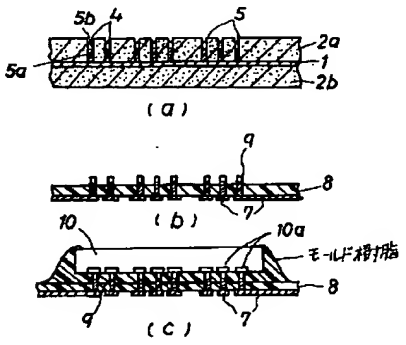
９……端子部　　10……ベアチップ　　10a……ベアチップの入出力端子

11……積層配線板　　12……多層型積層配線板　　13′……端子（テスト用）　　７……配線パターン　　８……ベアチップ

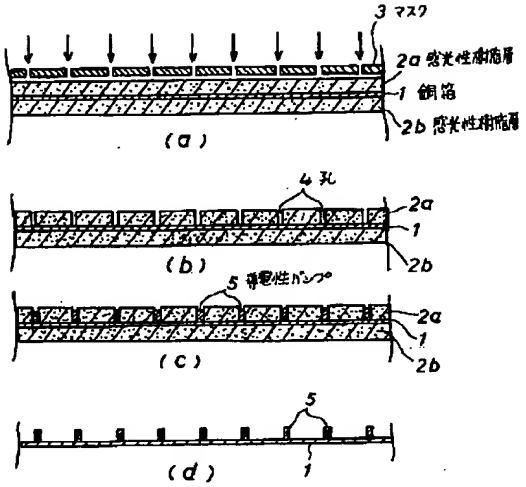
【図２】



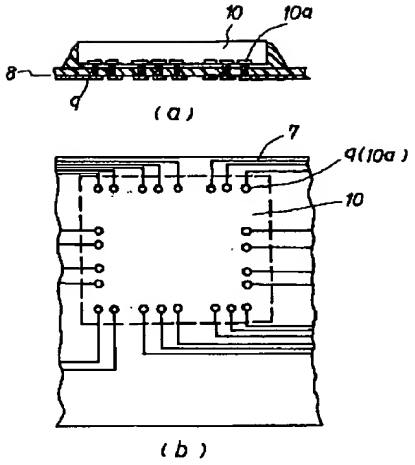
【図４】



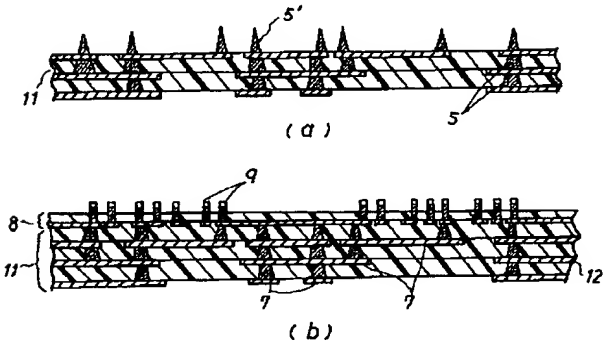
【図１】



【図３】



【図５】



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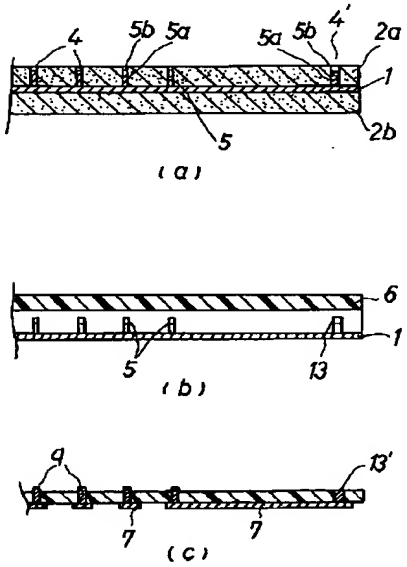

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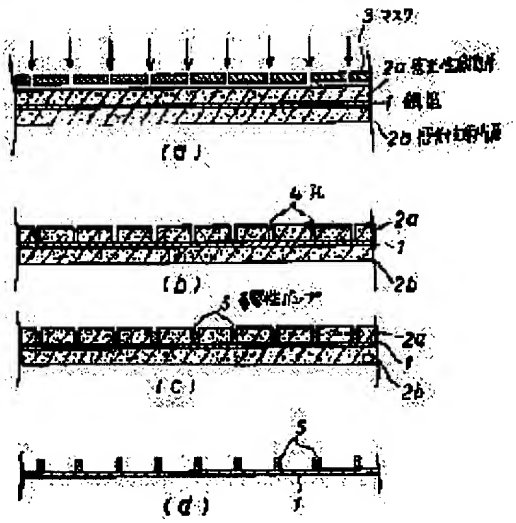
(54) MANUFACTURE OF MOUNTING PRINTED WIRING BOARD

(57)Abstract:
PURPOSE: To obtain a mounting wiring board equipped with fine terminals accurately located at prescribed positions by a method wherein the terminals electrically connected to the input/output terminals of electronic parts which are mounted on the board are selectively grown and formed through a plating method on the tips of conductive bumps that penetrate through an insulating layer.
CONSTITUTION: Photosensitive resist films 2a and 2b are pasted on both the sides of an electrolytic copper foil 1 respectively and irradiated with light rays through the intermediary of a mask 3, and holes 4 are provided in the resist film 2a by development. Thereafter the copper foil 1 is dipped into a copper electroplating solution and subjected to copper electroplating, whereby an electrolytic copper foil 1 where protrudent conductive bumps 5 are formed on one main surface is obtained. Then, a synthetic resin sheet, an aluminum foil, and a kraft paper are laminated on the electrolytic copper foil 1, which is pressed by a hot press into a laminate where the tips of the conductive bumps 5 are exposed on the outer surface of the synthetic resin sheet penetrating through it. Thereafter, a wiring is patterned by selective etching, etching resist is removed, and thus a mounting wiring board is obtained.



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CLAIMS

[Claim(s)]
[Claim 1] The process which arranges a photosensitive resist layer in the principal plane of a conductive metallic foil, and the process at which said photosensitive resist layer is exposed alternatively, carries out a development, and a conductive metallic foil side is exposed alternatively, The process which is made to carry out plating growth of the conductive metal, and forms a conductive bump on said exposed conductive metallic foil side, The process which exfoliates and removes the photosensitive resist layer of said conductive bump forming face, The process which piles up and carries out the laminating of the synthetic-resin system sheet to the conductive bump forming face of said conductive metallic foil, The process which said layered product is pressurized, and a conductive bump point is **** (ed) and exposed in the thickness direction of an insulating synthetic-resin sheet, and forms the terminal area for connection, The manufacture approach of the patchboard for mounting which carries out etching removal of said conductive metallic foil alternatively, and is characterized by providing the process which carries out wiring patterning and changing.
[Claim 2] Process which arranges a photosensitive resist layer in a circuit pattern formation principal plane The process at which said photosensitive resist layer is exposed alternatively, carries out a development, and a circuit pattern side is exposed alternatively, The process which is made to carry out plating growth of the conductive metal, and forms a conductive bump on said exposed circuit pattern side, The process which exfoliates and removes the photosensitive resist layer of said conductive bump forming face, The process which piles up and carries out the laminating of the synthetic-resin system sheet to the conductive bump forming face of said circuit pattern, The manufacture approach of the patchboard for mounting characterized by providing the process which said layered product is pressurized, and a conductive bump point is ****(ed) and exposed in the thickness direction of an insulating synthetic-resin sheet, and forms the terminal area for connection, and changing.
[Claim 3] The manufacture approach of claim 1 characterized by covering with the plating layer of a low contact resistance nature metal the terminal area side for connection ****(ed) and exposed, or the patchboard for mounting according to claim 2.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the manufacture approach of the patchboard for mounting, and the terminal area of the circuit pattern linked to the input/output terminal of mounting electronic parts is related with the manufacture approach of the patchboard for mounting drawn by the component side in more detail.
[0002]
[Description of the Prior Art] For example, practical use is presented with the mounting circuit apparatus which carries and mounts various kinds of electronic parts, such as a semiconductor device, at a patchboard, and changes widely as passive circuit elements of electronic equipment. And the so-called multilayer mold patchboard is used for the configuration of this kind of mounting circuit apparatus corresponding to the demand of the densification of a circuit, or miniaturization. More specifically, the high-density-assembly means which shortens a wire length is taken in electronic circuitries, such as a computer, so that high-speed signal propagation can be performed between semiconductor devices. That is, raising packaging density using a patchboard with small wiring width of face, while a semiconductor device is mounted with a bare chip and a component-side product is made small, a wire length is shortened and the densification of a circuit etc. is supported.
[0003] By the way, generally said multilayer mold patchboard is manufactured with the following means. namely, the wiring patterning side top after carrying out wiring patterning of the copper foil stretched to both sides of an insulating substrate, respectively -- an insulation sheet (for example, prepreg layer) -- minding -- copper foil -- a laminating -- it arranges and unifies by heating pressurization. subsequently, said layered product -- for example, a drill etc. -- a hole -- after performing dawn processing, the metal stratification of the internal surface of a hole is carried out with chemistry plating, and further, it thickness-attaches, it carries out by electroplating, and electrical installation between the wiring layers of a inner layer circuit pattern and an outer layer circuit pattern is performed. Then, about surface copper foil, wiring patterning containing a terminal area (pad for connection) was performed, and the multilayer mold patchboard has been obtained. In addition, in the case of the multilayer mold patchboard with more many circuit pattern layers, it is manufactured by the method which increases the number of double-sided mold patchboards made to insert in the middle.
[0004] Furthermore, the wiring substrate side which used the ceramics as the layer insulation body whorl as a multilayer mold patchboard with which a configuration differs from the above is presented also with the laminating and the patchboard of a configuration of having unified for mounting in the thin film multilayer-interconnection layer which uses for example, polyimide system resin as a layer insulation body whorl. Moreover, when a semiconductor device (LSI) is mounted in the multilayer mold printed circuit board manufactured by the above with a bare chip and it plans high density assembly to it, the bump was prepared in the input/output terminal side of a bare chip with solder, and it has connected with it with the terminal area (pad) of a multilayer mold printed circuit board side through this solder bump.
[0005]
[Problem(s) to be Solved by the Invention] However, with the mounting means of the bare chip through the above-mentioned solder bump, since the solder bump of the size ******** minute size of the input/output terminal of a bare chip who mounts is required, a solder bump's formation not only makes it complicated, but a problem is in the yield from points, such as a solder bump's configuration and size, and a location, precision. On the other hand, in a patchboard, not only narrow-izing of wiring width of face but micrifying of the terminal area (pad) which connects the input/output terminal of a bare chip or narrow-izing between terminal areas (pad) is required corresponding to high-density-assembly-izing. And in this multilayer mold patchboard, since NC drill machine processing cannot be applied

when there is a limitation also in the diameter of SURUHORU which connects between circuit pattern layers naturally and it sets the diameter of SURUHORU as the diameter of about 0.10mm for example, if the improvement in said wiring consistency and improvement in packaging density are taken into consideration, new processing equipment or a processing means will be required separately. Anyway, in the case of the multilayer mold patchboard of a configuration of being known conventionally, or the multilayer mold patchboard formed with the conventional manufacture means, there is a problem after the densification of a mounting circuit apparatus, or miniaturization.

[0006] This invention coped with the above-mentioned situation, was made, and aims at offer of the manufacture approach of the patchboard for mounting which made possible reliable high density wiring and high density assembly.

[0007]

[Means for Solving the Problem] The manufacture approach of the 1st patchboard for mounting concerning this invention The process which arranges a photosensitive resist layer in the principal plane of a conductive metallic foil, and the process at which said photosensitive resist layer is exposed alternatively, carries out a development, and a conductive metallic foil side is exposed alternatively, The process which is made to carry out plating growth of the conductive metal, and forms a conductive bump on said exposed conductive metallic foil side, The process which exfoliates and removes the photosensitive resist layer of said conductive bump forming face, The process which piles up and carries out the laminating of the synthetic-resin system sheet to the conductive bump forming face of said conductive metallic foil, It is characterized by providing the process which said layered product is pressurized, and a conductive bump point is ****(ed) and exposed in the thickness direction of an insulating synthetic-resin sheet, and forms the terminal area for connection, and the process which carries out etching removal of said conductive metallic foil alternatively, and carries out wiring patterning, and changing. Moreover, the manufacture approach of the 2nd patchboard for mounting concerning this invention The process which arranges a photosensitive resist layer in a circuit pattern formation principal plane, and the process at which said photosensitive resist layer is exposed alternatively, carries out a development, and a circuit pattern side is exposed alternatively, The process which is made to carry out plating growth of the conductive metal, and forms a conductive bump on said exposed circuit pattern side, The process which exfoliates and removes the photosensitive resist layer of said conductive bump forming face, It is characterized by providing the process which piles up and carries out the laminating of the synthetic-resin system sheet to the conductive bump forming face of said circuit pattern, and the process which said layered product is pressurized, and a conductive bump point is ****(ed) and exposed in the thickness direction of an insulating synthetic-resin sheet, and forms the terminal area for connection, and changing.

[0008] Furthermore, in the above-mentioned manufacture approach, it is desirable to cover with the plating layer of a low contact resistance nature metal the terminal area side for connection which ****(ed) and exposed the synthetic-resin system sheet by pressurization of a layered product.

[0009] In this invention, a conductive bump is formed of alternative plating of conductive metals, such as copper. And in order to enable arbitrary formation of a conductive bump [pitch still more minutely] highly precise and minute as mask material for performing this alternative plating, a photopolymer is chosen, and arrangement of this photopolymer is performed by spreading, desiccation, etc. of the lamination of a photopolymer film, or a photopolymer solution.

[0010] moreover, since the conductive bump of the letters of a projection (for example, the shape of a cone, a pillar-shaped object, etc.) formed with the plating of said conductive metal is selected as the thickness of the mask which said photopolymer layer accomplishes, the path of the hole prepared in the mask, distribution, etc. 4, she is suitably set up according to the configuration of the **** type terminal area (pad) to form and the connection between circuit pattern layers.

[0011] The point of the conductive bump of said letter of a projection is ****(ed), a thermoplastics film (sheet) is mentioned, for example as a synthetic-resin system sheet which forms a terminal area and the interlayer connection section, and the thickness is 25 to 300 micrometer. Extent is desirable. Here, as a thermoplastics sheet, sheets, such as 6 4 fluoride [polycarbonate resin, polysulfone resin, thermoplastic polyimide resin, and polyethylene resin] and polypropylene resin fluoride and polyether ether ketone resin, are mentioned, for example. Moreover, as a thermosetting resin sheet held at the condition before hardening, the sheets of crude rubber, such as an epoxy resin, bismaleimide triazine resin, polyimide resin, phenol resin, polyester resin, melamine resin or swine JIENGOMU, isobutylene isoprene rubber, natural rubber, neoprene rubber, and silicone rubber, are mentioned. These synthetic resin may be sheets which may contain an insulating inorganic substance and packing of an organic substance system although it may be independent, and change combining reinforcing materials, such as glass fabrics, a mat, organic synthesis fiber cloth and a mat, or paper, further.

[0012] Moreover, in making a synthetic-resin system sheet front face **** and expose said conductive bump's point, and forming a terminal area (pad), it is desirable to take the following means. Namely, make a synthetic-resin system

sheet principal plane opposite-** to the base side which made the conductive bump of the letter of a projection, and laminating arrangement is carried out to it. On both sides of this layered product, metal plates, such as a stainless plate, a brass plate, etc. with little the dimension and deformation as a corrosion plate, For example, heat-resistant-resin plates, such as a polyimide resin plate (sheet) and a polytetrafluoroethylene resin plate (sheet), are arranged and pressurized, and it can form by making the conductive bump tip side of the letter of a projection **** in the thickness direction of a synthetic-resin system sheet.

[0013]

[Function] According to the manufacture approach of the patchboard for mounting concerning this invention, the terminal area (pad) electrically connected with the input/output terminal of the electronic parts to mount is formed by the point of the conductive bump who was alternatively grown up and formed by the so-called galvanizing method, and ****(ed) the insulator layer. That is, a terminal area (pad) takes the configuration exposed to a patchboard side in an embedding derivation form, and is not only being formed in a highly precise dimension and a configuration (dispersion in height being ** 2micrometer extent) but 300 micrometer. It can arrange in the pitch below extent (for example, 100micrometer extent). And in connection with the ability to install said conductive bump in a detailed configuration and a minute pitch, the patchboard with which improvement in a wiring consistency and packaging density was also achieved collectively will be obtained. And since SURUHORU does not exist in a patchboard side, reduction of the feeder-line field and a mounting field will also be canceled at least, it will be promoted further and improvement in said wiring consistency and packaging density can offer the reliable patchboard for mounting with the sufficient yield.

[0014]

[Example] The following, drawing 1 (a) - (d), drawing 2 (a) - (c), drawing 3 (a), (b), drawing 4 (a) - (c), drawing 5 (a), (b) and drawing 6 (a) - The example of this invention is explained with reference to (c).

[0015] Example 1 drawing 1 (a) - (d) and drawing 2 (a) - (c) shows typically the example of a mode of the manufacture approach of the patchboard for mounting by this example.

[0016] 18 micrometers in first, thickness currently used for manufacture of a printed circuit board 150 micrometers in electrolytic copper foil and thickness The photopolymer film (trade name-hotec SR-3000EB-22 product made from Hitachi Chemical KK) was prepared. And drawing 1 As shown in (a) in cross section, after making said photopolymer (photosensitive resist) film 2a and 2b rival to both sides of said electrolytic copper foil 1, respectively, light was irradiated through the mask 3 to them at photosensitive resist film 2a (alternative exposure). Subsequently, a development is performed about said photosensitive resist film 2a which carried out alternative exposure, and 2b, and it is drawing 1 . As shown in (b) in cross section, it is the diameter of about 75 micrometers to photosensitive resist film 2a. The hole 4 was formed.

[0017] Then, it is immersed by using said electrolytic copper foil 1 as cathode into electrolytic copper plating liquid (trade name: KC500 product made from Japan Energy KK), electrolytic copper plating processing is performed, and it is drawing 1 . As shown in (c) in cross section, it is height in the hole 4 of said photosensitive resist film 2a (alternative exposure of electrolytic copper foil 1). 130 micrometers The copper of extent was grown up. Photopolymer film 2a operated as a mask and 2b are exfoliated after said plating processing termination, and it is drawing 1 . As shown in (d) in cross section, conductive bump 5 group of the letter of a projection obtained the electrolytic copper foil 1 formed in one principal plane. Next, it is drawing 2 to the letter conductivity bump of projection 5 group forming face of said electrolytic copper foil 1. As shown in (a) in cross section, it is 50 micrometers in thickness. Laminating arrangement of the synthetic-resin sheet 6, for example, Teflon-resin-glass-fabrics system prepreg, and the aluminum foil which is not illustrated, and the kraft paper was carried out. This layered product is set between the hot platens of the heat press machine held at 180 degree C, and it pressurizes by about 1.96x106Pa, holds for 15 minutes as it is, and is drawing 2 (b). The laminate which conductive bump 5 point as shown in cross section ****(ed) six layers of synthetic-resin sheets, and was exposed to other fields was obtained. Then, after printing etching resist to the 1st page of the electrolytic copper foil of said laminate, performing alternative etching of the electrolytic copper foil 1 and taking wiring patterning 7, exfoliation removal of said etching resist is carried out in an alkali water solution, and it is drawing 2 (c). The patchboard 8 for mounting as shown in cross section was obtained.

[0018] It sets to said patchboard 8 for mounting, and is drawing 2 . As shown in (c) in cross section, the conductive bump's 5 point was exposed to one principal plane (front face) as a terminal area (pad) 9, and the configuration that the circuit pattern 7 connected with a terminal area 9 at the principal plane (rear face) of another side was made is accomplished to it. and it is set as said terminal area 9 predetermined location -- having -- **** -- drawing 3 Cross-section-[(a)] and drawing 3 it is shown in (b) in flat-surface fluoroscopy -- as -- for example, -- Input/output terminal of the LSI (semi-conductor) bare chip 10 It opposite-**(ed) certainly with 10a, and the electric connection stabilized by junction between metals (association of metals and metal ordinary temperature junction are included) was made.

[0019] Example 2 drawing 4 (a) - (c) shows typically the example of a mode of the manufacture approach of the patchboard for mounting by this example.
[0020] 18 micrometers in first, thickness currently used for manufacture of a printed circuit board 150 micrometers in electrolytic copper foil and thickness The photopolymer film (trade name-hotec SR-3000EB-22 product made from Hitachi Chemical KK) was prepared. And after making said photopolymer (photosensitive resist) film 2a and 2b rival to both sides of said electrolytic copper foil 1, respectively, light was irradiated through the mask to them at photosensitive resist film 2a (alternative exposure). Subsequently, a development is performed about said photosensitive resist film 2a which carried out alternative exposure, and 2b, and it is the diameter of about 75 micrometers to photosensitive resist film 2a. The hole 4 was formed.
[0021] Then, it is immersed by using said electrolytic copper foil 1 as cathode into electrolytic copper plating liquid (trade name: KC500 product made from Japan Energy KK). Electrolytic copper plating processing and gilding processing are performed one by one, and it is drawing 4 . As shown in (a) in cross section In the hole 4 of said photosensitive resist film 2a (alternative exposure of electrolytic copper foil 1), it is height. 130 micrometers Copper 5a of extent is grown up and it is height of 15 micrometers on it further. The laminating of the golden 5b of extent was carried out. Photopolymer film 2a operated as a mask and 2b were exfoliated after said plating processing termination, and letter conductivity bump of projection 5 group of the form where the laminating of copper 5a and the golden 5b was carried out obtained the electrolytic copper foil 1 formed in one principal plane.
[0022] Next, it is 50 micrometers in thickness to the letter conductivity bump of projection 5 group forming face of said electrolytic copper foil 1. Laminating arrangement of the synthetic-resin sheet 3, for example, Teflon-resin-glass-fabrics system prepreg, and aluminum foil and kraft paper was carried out. This layered product was set between the hot platens of the heat press machine held at 180 degree C, and it pressurized by abbreviation 1.96x106 Pa, and held for 15 minutes as it is, and the laminate which conductive bump 5 point ****(ed) six layers of synthetic-resin sheets, and was exposed to other fields was obtained. Then, after printing etching resist to the 1st page of the electrolytic copper foil of said laminate, performing alternative etching of the electrolytic copper foil 1 and taking wiring patterning 7, exfoliation removal of said etching resist was carried out in the alkali water solution, and the patchboard 8 for mounting was obtained.
[0023] It sets to said patchboard 8 for mounting, and is drawing 4 . As shown in (b) in cross section, the conductive bump's 5 point was exposed to one principal plane (front face) as a terminal area (pad) 9, and the configuration that the circuit pattern 7 connected with a terminal area 9 at the principal plane (rear face) of another side was made is accomplished to it. and it is set as said terminal area 9 high degree of accuracy in a predetermined location -- having -- **** -- drawing 4 it is shown in (c) in cross section -- as -- for example, -- Input/output terminal of the LSI (semi-conductor) bare chip 10 It opposite-**(ed) certainly with 10a, and the electric connection stabilized by junction between metals was made.
Example 3 drawing 5 (a) It reaches. (b) is the sectional view showing typically other examples of a mode of the manufacture approach of the patchboard for mounting by this example.
[0024] 18 micrometers in first, thickness currently used for manufacture of a printed circuit board Electrolytic copper foil, a polymer type silver system paste (trade name: product made from KEMITAITO MS-89. Toshiba Chemical KK), thickness 100 micrometers In the predetermined location of a stainless steel plate The metal mask which ends and changes the hole of the diameter of 0.1mm was prepared, respectively. And to said electrolytic-copper-foil side, positioning arrangement of the metal mask is carried out, a silver system paste is printed, and it is min to a rectangle mostly about the conductive bump of the letter of a projection. Covering formation was carried out in the pitch of about 0.3mm. the approach of printing again in the same location after said conductive bump who printed drying using the same metal mask -- 4 times -- repeating -- conductive bump formation of the shape of an approximate circle drill of 60 to 100 micrometer height -- it carried out.
[0025] Subsequently, it is 50 micrometers in thickness to the conductive bump forming face side of said electrolytic copper foil. A synthetic-resin sheet, for example, Teflon-resin-glass-fabrics system prepreg, is minded, and it is 18 micrometers in thickness. Laminating arrangement of the electrolytic copper foil was carried out. This layered product is set between the hot platens of the heat press machine held at 180 degree C, and it pressurizes by abbreviation 1.96x106 Pa, holds for 15 minutes as it is, and is drawing 4 (b). The laminate to which between the electrolytic-copper-foil sides where a conductive bump's point as shown in cross section **** a synthetic-resin sheet layer, and counters was connected electrically was obtained.
[0026] Subsequently, etching resist was printed to the 1st page of both the electrolytic copper foil of said laminate, after performing and carrying out wiring patterning of the alternative etching of the electrolytic copper foil 1, exfoliation removal of said etching resist was carried out in the alkali water solution, and the double-sided mold patchboard was

obtained. 18 micrometers in thickness which minds [of one circuit pattern side of this double-sided mold patchboard / predetermined] formation of the conductive bump of a silver paste system, for example, Teflon-resin-glass-fabrics system prepreg, according to said technique Laminating unification of electrolytic copper foil and wiring patterning of this electrolytic copper foil are repeated, and it is drawing 5 . The laminating patchboard 11 as shown in (a) in cross section was created.

[0027] To the conductive bump 5' forming face of said created laminating patchboard 11, it is 50 micrometers in thickness. Teflon-resin-glass-fabrics system prepreg is minded, for example, and it is said drawing 4 . Laminating arrangement of the patchboard 8 for mounting illustrated to (b) was carried out. This layered product is set between the hot platens of the heat press machine held at 180 degree C. While pressurizing by abbreviation 1.96x106 Pa, holding for 15 minutes as it is, and a conductive bump 5' point's ****(ing) six layers of synthetic-resin sheets and connecting with the wiring putter 7 of the patchboard 8 for mounting electrically The patchboard 12 for mounting of the multilayer mold with which the patchboard 8 for mounting and the laminating patchboard 11 carry out laminating unification, and change was obtained.

[0028] In said multilayer type of patchboard 12 for mounting, the configuration which the conductive bump's 5 point exposed to one principal plane (front face) as a terminal area (pad) 9 is accomplished. and -- since it is arranged in said terminal area 9 predetermined location with a sufficient precision -- for example -- the input/output terminal of an LSI (semi-conductor) bare chip -- ** -- it opposite-**(ed) certainly and the electric connection stabilized by junction between metals was made.

[0029] Example 4 drawing 6 (a) - (c) shows typically the example of a mode of the manufacture approach of the patchboard for mounting by this example.

[0030] 18 micrometers in first, thickness currently used for manufacture of a printed circuit board 150 micrometers in electrolytic copper foil and thickness The photopolymer film (trade name-hotec SR-3000EB-22 product made from Hitachi Chemical KK) was prepared. And after making said photopolymer (photosensitive resist) film 2a and 2b rival to both sides of said electrolytic copper foil 1, respectively, light was irradiated through the mask 3 to them at photosensitive resist film 2a (alternative exposure). in addition, this alternative exposure processing -- setting -- the object for a circuit tester's BUROBU contact -- a conductor -- the exposure for installing in a periphery was also combined and the bump 13 was performed.

[0031] Subsequently, a development is performed about said photosensitive resist film 2a which carried out alternative exposure, and 2b, and it is the diameter of about 75 micrometers to photosensitive resist film 2a. A hole 4 and 4' were prepared.

[0032] Then, it is immersed by using said electrolytic copper foil 1 as cathode into electrolytic copper plating liquid (trade name: KC500 product made from Japan Energy KK). Electrolytic copper plating processing and gilding processing are performed one by one, and it is drawing 6 . As shown in (a) in cross section In the hole 4 of said photosensitive resist film 2a (alternative exposure of electrolytic copper foil 1) Height 130 micrometers Copper 5a of extent is grown up and it is height of 15 micrometers on it further. The laminating of the golden 5b of extent is carried out. moreover, a hole -- the inside (similarly alternative exposure of electrolytic copper foil 1) of 4' -- height 150 to 200 micrometer copper 5a of extent is grown up -- making -- further -- a it top -- height of 15 micrometers The laminating of the golden 5b of extent was carried out. Photopolymer film 2a operated as a mask and 2b were exfoliated after said plating processing termination, and the letter conductivity bump 5 of a projection of the form where the laminating of copper 5a and the golden 5b was carried out, and 13 groups obtained the electrolytic copper foil 1 formed in one principal plane.

[0033] Subsequently, drawing 6 (b) 50 micrometers in thickness which constitutes a substrate body to conductive bump [of said electrolytic copper foil 1] 5, and 13 forming-face side so that it may be shown in cross section Laminating arrangement of the Teflon-resin-glass-fabrics system prepreg 6 was carried out. This layered product was set between the hot platens of the heat press machine held at 180 degree C, and it pressurized by abbreviation 1.96x106 Pa, and held for 15 minutes as it is, and the laminate which the conductive bumps' 5 and 13 point ****(ed) six layers of synthetic-resin sheets, and was exposed to other fields was obtained.

[0034] Furthermore, the conductive bump 13 with height high among the conductive bumps 5 and 13 who have ****** (ed) and exposed said laminate on the other hand was crushed and processed with the press machine. Subsequently, etching resist is printed to the 1st page of the electrolytic copper foil of said laminate, after performing and carrying out wiring patterning of the alternative etching of the electrolytic copper foil 1, exfoliation removal of said etching resist is carried out in an alkali water solution, and it is drawing 6 (c). Patchboard 8' for mounting as shown in cross section was obtained.

[0035] Input/output terminal of the bare chip 10 mounted in the patchboard for mounting of said configuration Since

terminal 13' electrically connected to the terminal area 9 linked to 10a is drawn by the periphery, after carrying and mounting a bare chip 10, it is possible to perform easily the test of loading, the good of the mounted bare chip 10, and a defect using terminal 13' which said periphery was made to draw. That is, it is the input/output terminal of a bare chip 10 about a circuit tester's probe. Depending on the design of the wiring putter 7 which connects between the terminal area 9 which can ensure [easily] property investigation of the bare chip 10 which was not directly contacted to 10a and also mounted **, and the conductive bumps 5 and 13 form, and terminal 13', the characterization in two or more circuit testers' probe is also possible. In addition, this invention is not limited to the above-mentioned example, and can take various deformation in the range which does not deviate from the meaning of invention. For example, as an insulator between circuit pattern layers, polyimide resin, polysulphone resin, etc. may be used instead of a Teflon-resin-glass-fabrics system.

[0036]

[Effect of the Invention] According to the manufacture approach of the patchboard for mounting concerning this invention, it becomes possible to obtain easily the patchboard for mounting which took the configuration equipped with the minute terminal area (pad) with a precision sufficient in a predetermined location so that clearly from explanation of the above-mentioned example etc. For example, dispersion in the height of said terminal area is also ** 2micrometer. Also connection resistance [in / it is below extent and / a terminal area] It is 0.1ohms or less and is a terminal area further. 100 micrometers It can arrange in the pitch of extent. And since highly precise-ization of the setting location of a terminal area or a configuration in said patchboard for mounting can also perform alignment with the input/output terminal to which a bare chip corresponds, and connection, offer of a reliable mounting circuit apparatus is attained. Moreover, since complicated processing, such as SURUHORU drilling and SURUHORU plating, not only becomes unnecessary, but surface derivation of said terminal area is a conductive bump's ****, it is the so-called flush type and constraint of the wiring field by said SURUHORU and a mounting field is reduced, wiring-izing and mounting-izing of high density are attained.

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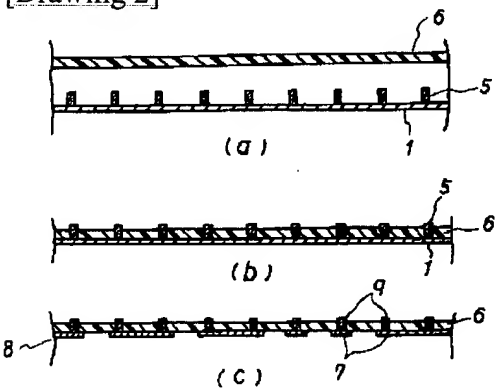
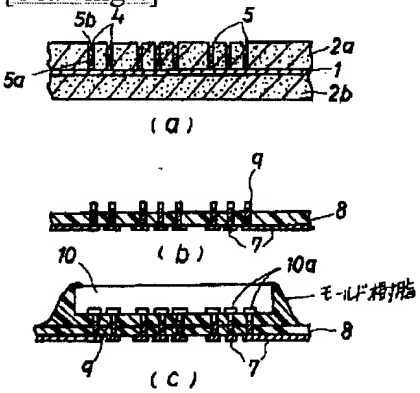
DRAWINGS

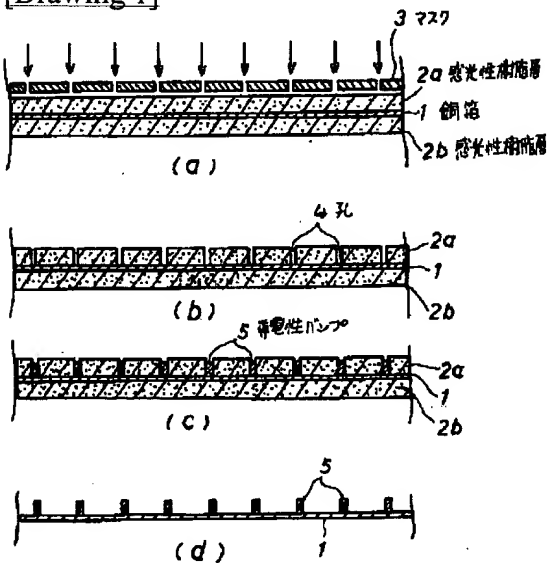
[Drawing 2]



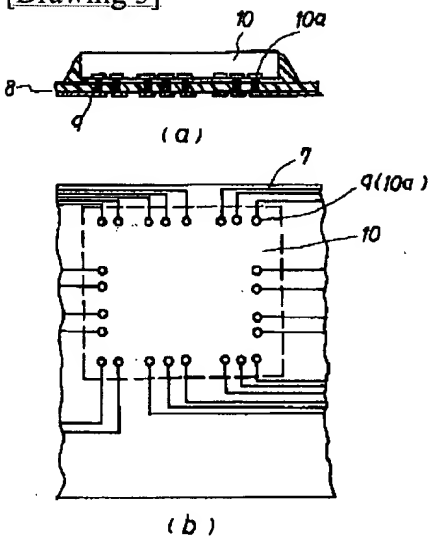
[Drawing 4]



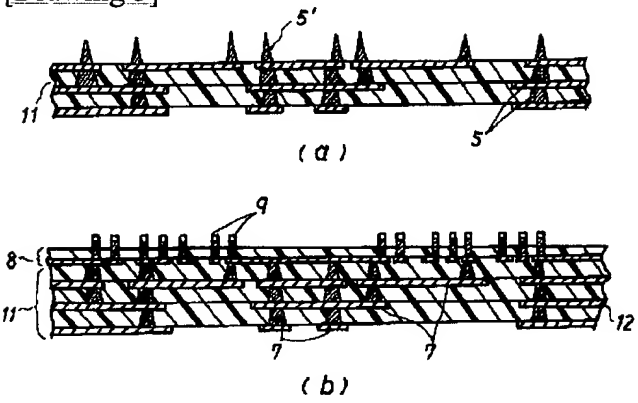
[Drawing 1]



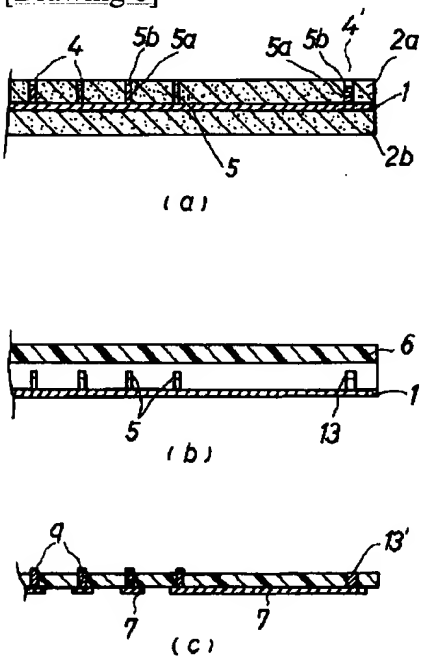
[Drawing 3]



[Drawing 5]



[Drawing 6]



[Translation done.]

* NOTICES *.

CORRECTION OR AMENDMENT

[Kind of official gazette] Printing of amendment by the convention of 2 of Article 17 of Patent Law
[Section partition] The 2nd partition of the 7th section
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3/06 H
A
3/24 A

[Procedure revision]
[Filing Date] January 19, Heisei 13 (2001. 1.19)
[Procedure amendment 1]
[Document to be Amended] Specification
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[Proposed Amendment]
[Claim(s)]
[Claim 1] The process which arranges a photosensitive resist layer in the principal plane of a conductive metallic foil,
The process at which said photosensitive resist layer is exposed alternatively, carries out a development, and a conductive metallic foil side is exposed alternatively,
The process which is made to carry out plating growth of the conductive metal, and forms a conductive bump on said exposed conductive metallic foil side,
The process which exfoliates and removes the photosensitive resist layer of said conductive bump forming face,
The process which piles up and carries out the laminating of the synthetic-resin system sheet to the conductive bump forming face of said conductive metallic foil,
The process which said layered product is pressurized, and a conductive bump point is penetrated and exposed in the thickness direction of an insulating synthetic-resin sheet, and forms the terminal area for connection,
The manufacture approach of the patchboard for mounting which carries out etching removal of said conductive metallic foil alternatively, and is characterized by providing the process which carries out wiring patterning and changing.
[Claim 2] The process which arranges a photosensitive resist layer in a circuit pattern formation principal plane,

The process at which said photosensitive resist layer is exposed alternatively, carries out a development, and a circuit pattern side is exposed alternatively,
The process which is made to carry out plating growth of the conductive metal, and forms a conductive bump on said exposed circuit pattern side,
The process which exfoliates and removes the photosensitive resist layer of said conductive bump forming face,
The process which piles up and carries out the laminating of the synthetic-resin system sheet to the conductive bump forming face of said circuit pattern,
The manufacture approach of the patchboard for mounting characterized by providing the process which said layered product is pressurized, and a conductive bump point is penetrated and exposed in the thickness direction of an insulating synthetic-resin sheet, and forms the terminal area for connection, and changing.
[Claim 3] The manufacture approach of claim 1 characterized by covering with a low contact resistance nature metal plating layer the terminal area side for connection penetrated and exposed, or the patchboard for mounting according to claim 2.
[Claim 4] The process which arranges a photosensitive resist layer in the principal plane of a conductive metallic foil,
The process which exposes said photosensitive resist layer alternatively, carries out a development, is made to expose a conductive metallic foil side alternatively, and forms a hole in said photosensitive resist layer,
The process which is made to carry out plating growth of the conductive metal, and forms a conductive bump on said exposed conductive metallic foil side,
The process which exfoliates and removes the sensitization layer which remains in the principal plane of said conductive metallic foil,
The process which piles up and carries out the laminating of the insulating synthetic-resin sheet to the conductive bump forming face of said conductive metallic foil,
The process which said layered product is pressurized in the thickness direction, and a conductive bump point is penetrated and exposed in the thickness direction of said 1st insulating synthetic-resin sheet, and forms the terminal area for connection,
The manufacture approach of the high density patchboard for mounting which carries out etching removal of said conductive metallic foil alternatively, and is characterized by providing the process which forms a circuit pattern and changing.
[Claim 5] The process which arranges a photosensitive resist layer in the front face of the patchboard which has a circuit pattern,
The process which exposes said photosensitive resist layer alternatively, carries out a development, is made to expose the front face of said circuit pattern alternatively, and forms a hole in said photosensitive resist layer,
The process which is made to carry out plating growth of the conductive metal, and forms a conductive bump on said exposed circuit pattern,
The process which exfoliates and removes the sensitization layer which remains in the principal plane of said patchboard,
The process which piles up and carries out the laminating of the insulating synthetic-resin sheet to said conductive bump forming face,
The manufacture approach of the high density patchboard for mounting characterized by providing the process which said layered product is pressurized in the thickness direction, and a conductive bump point is penetrated and exposed in the thickness direction of said insulating synthetic-resin sheet, and forms the terminal area for connection, and changing.

[Claim 6] The process which arranges a photosensitive resist layer in the front face of the patchboard which has a circuit pattern,
The process which exposes said photosensitive resist layer alternatively, carries out a development, is made to expose the front face of said circuit pattern alternatively, and forms a hole in said photosensitive resist layer,
The process which is made to carry out plating growth of the conductive metal, and forms a conductive bump on said exposed circuit pattern,
The process which exfoliates and removes the sensitization layer which remains in the principal plane of said patchboard,
The process which arranges liquefied insulation synthetic resin in said conductive bump forming face,
The manufacture approach of the high density patchboard for mounting characterized by providing the process which said layered product is pressurized in the thickness direction, and a conductive bump point is penetrated and exposed in the thickness direction of said insulating synthetic resin, and forms the terminal area for connection, and changing.

[Claim 7] The process which forms a sensitization layer in the front face of a conductive foil,
The process which exposes said sensitization layer alternatively, carries out a development, is made to expose each field side of a conductive foil alternatively, and forms a hole in said sensitization layer,
The process which forms the 1st conductive metal on said exposed conductive foil surface, and forms a conductive bump,
The process which forms the 2nd conductive metal on said conductive bump,
The process which removes said sensitization layer from the front face of said conductive foil,
The process which piles up said insulating synthetic-resin sheet on said conductive bump so that said conductive bump point may project an insulating synthetic-resin sheet,
The manufacture approach of the patchboard which carries out patterning of said conductive foil, and is characterized by providing the process which forms a circuit pattern and changing.
[Claim 8] The process which forms a sensitization layer in the front face of a conductive foil,
The process which exposes said sensitization layer alternatively, carries out a development, is made to expose each field side of a conductive foil alternatively, and forms a hole in said sensitization layer,
The process which forms the 1st conductive metal on said exposed conductive foil surface, and forms a conductive bump,
The process which forms the 2nd conductive metal for forming said conductive bump's connection on said conductive bump,
The process which removes said sensitization layer from the front face of said conductive foil,
The process which piles up said insulating synthetic-resin sheet and forms a connection terminal area on said conductive bump so that said conductive bump point may project an insulating synthetic-resin sheet,
The process which carries out patterning of said conductive foil, and forms a circuit pattern,
The process which arranges the chip which has a connection electrode on said insulating synthetic-resin sheet so that said connection electrode may face said connection terminal area,
The manufacture approach of the semiconductor package which carries out pressurization heating of said circuit pattern, said insulating synthetic-resin sheet, and said chip, and is characterized by providing the process which connects the connection electrode of said chip to said connection terminal area electrically, and changing.
[Claim 9] The process which arranges a photosensitive resist layer in the principal plane of a conductive metallic foil,
The process which exposes said photosensitive resist layer alternatively, carries out a development, is made to expose a conductive metallic foil side alternatively, and forms a hole in said photosensitive resist layer,
The process which is made to carry out plating growth of the conductive metal, and forms a conductive bump on said exposed conductive metallic foil side,
The process which exfoliates and removes the sensitization layer which remains in the principal plane of said conductive metallic foil,
The process which piles up and carries out the laminating of the 1st insulating synthetic-resin sheet to the conductive bump forming face of said conductive metallic foil,
The process which said layered product is pressurized in the thickness direction, and a conductive bump point is penetrated and exposed in the thickness direction of said 1st insulating synthetic-resin sheet, and forms the terminal area for connection,
The process which forms the 1st patchboard which carries out etching removal of said conductive metallic foil alternatively, and has the 1st circuit pattern,
The process which piles up and carries out the laminating of said 1st patchboard through the 2nd insulating synthetic-resin sheet on the 2nd [of the 2nd patchboard] circuit pattern which has the 2nd conductive bump in a predetermined location,
The manufacture approach of the high density patchboard for mounting characterized by providing the process which said layered product is pressurized in the thickness direction, and said 2nd conductive bump point is penetrated and exposed in the thickness direction of said 2nd insulating synthetic-resin sheet, and is connected with the 1st circuit pattern of said 1st patchboard, and changing.
[Claim 10] Said 2nd patchboard is the manufacture approach of the high density patchboard for mounting according to claim 9 characterized by being a multilayer-interconnection plate.
[Claim 11] The manufacture approach of said 2nd patchboard of said multilayer-interconnection plate,
The 1st process which forms said conductive bump by arranging the metal mask which has a hole for the conductive bump of the predetermined location of the front face of the 1st conductive metallic foil, and repeating printing and desiccation of the conductive paste on said front face,

The 2nd process which piles up a resin sheet and the 2nd conductive metallic foil one by one on the front face which has said conductive bump,
The 3rd process which forms the laminating sheet which heating pressurization of said layered product is carried out at coincidence, said conductive bump's point penetrates said resin sheet, connects with said 2nd conductive metallic foil, and has the 1st conductive metallic foil side and the 2nd conductive metallic foil side,
It has the 4th process which prints an etching-resist layer, etches alternatively said the 1st and said 2nd conductive metallic foil, forms a circuit pattern on said 1st conductive metallic foil side and said 2nd conductive metallic foil side, removes said etching-resist layer and forms a double-sided patchboard,
The manufacture approach of the high density patchboard for mounting according to claim 10 characterized by forming a multilayer-interconnection plate by repeating said 1st, 2nd, 3rd, and 4th process two or more times.

[Translation done.]